CMOS Digital Integrated Circuits Silicon Monolithic

74VHC540FT,74VHC541FT

1. Functional Description

- Octal Bus Buffer

74VHC540FT: Inverted, 3-State Outputs
74VHC541FT: Non-Inverted, 3-State Outputs

2. General

The 74VHC540FT/74VHC541FT are advanced high speed CMOS OCTAL BUS BUFFERs fabricated with silicon gate C^2MOS technology.

They achieve the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

The 74VHC540FT is an inverting type, and the 74VHC541FT is a non-inverting type.

When either $\overline{G}1$ or $\overline{G}2$ are high, the terminal outputs are in the high-impedance state.

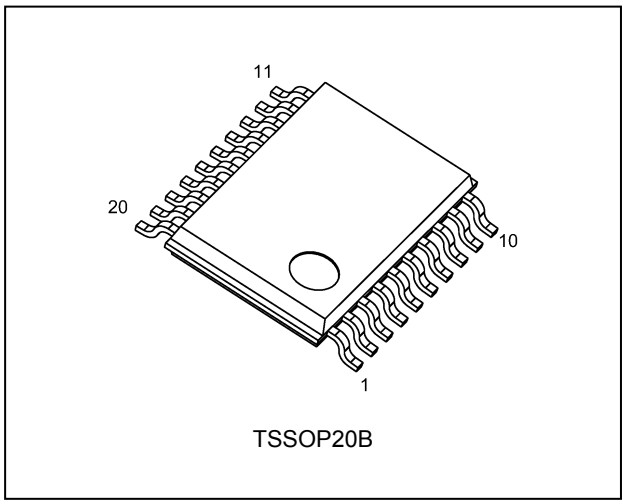
An input protection circuit ensures that 0 to 5.5 V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5 V to 3 V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages

3. Features

(1) AEC-Q100 (Grade 1) qualified. (Note 1)
(2) Wide operating temperature : T_{opr} = -40℃ to 125 ℃
(3) High speed: Propagation delay time = 3.7 ns (typ.) at V_{CC} = 5 V
(4) Low power dissipation: I_{CC} = 4 μA (max) at T_a = 25 ℃
(5) High noise immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC} (min)
(6) Power down protection is provided on all inputs.
(7) Balanced propagation delays: $t_{PLH} \approx t_{PHL}$
(8) Wide operating voltage range: $V_{CC(opr)}$ = 2 V to 5.5 V
(9) Low noise: V_{OLP} = 1.0 V (max)
(10) Pin and function compatible with 74 series (74AC/HC/AHC/LV etc.) 540 or 541 type.

Note 1: For detail information, Please contact to our sales.

4. Packaging

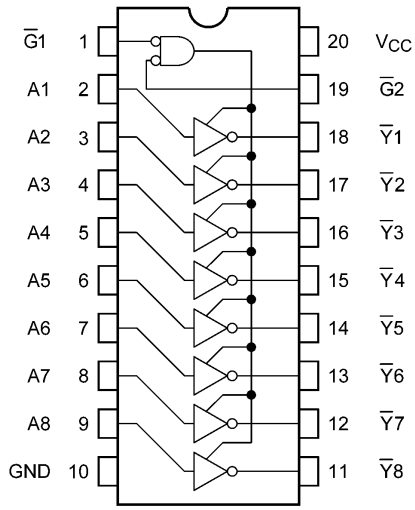


TSSOP20B

Start of commercial production
2013-03

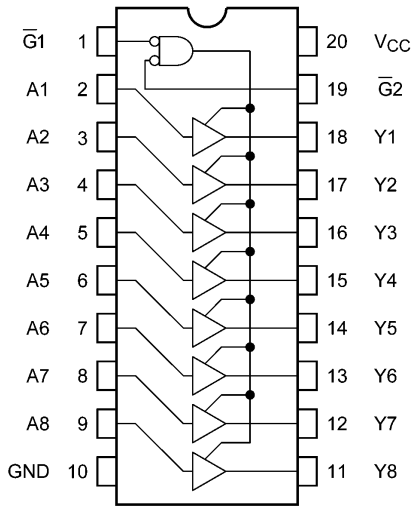
5. Pin Assignment

74VHC540FT



(top view)

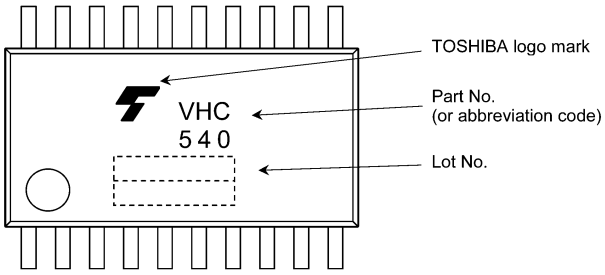
74VHC541FT



(top view)

6. Marking

74VHC540FT



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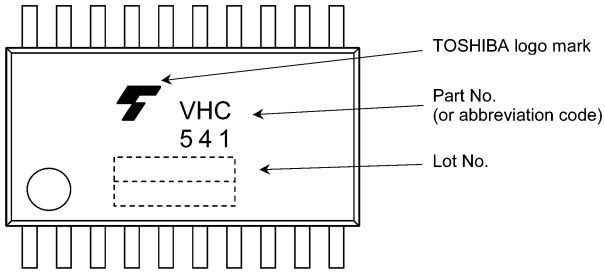
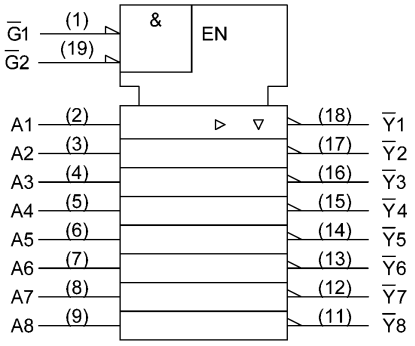
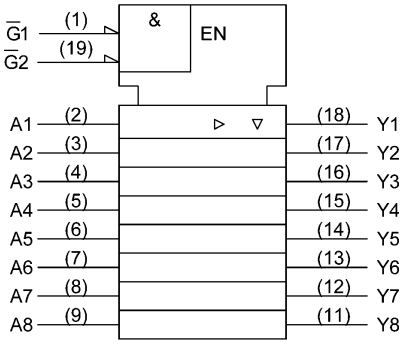


7. IEC Logic Symbol

74VHC540FT



74VHC541FT



8. Truth Table

Input $\overline{G}1$	Input $\overline{G}2$	Input A_n	Output Y_n	Output $\overline{Y}_n$
H	X	X	Z	Z
X	H	X	Z	Z
L	L	H	H	L
L	L	L	L	H

X: Don't care
Z: High impedance
Y_n: 74VHC541FT
$\overline{Y}_n$: 74VHC540FT

9. Absolute Maximum Ratings (Note)

Characteristics	Symbol	Note	Rating	Unit
Supply voltage	V_{CC}		-0.5 to 7.0	V
Input voltage	V_{IN}		-0.5 to 7.0	V
Output voltage	V_{OUT}		-0.5 to V_{CC} + 0.5	V
Input diode current	I_{IK}		-20	mA
Output diode current	I_{OK}		±20	mA
Output current	I_{OUT}		±25	mA
V_{CC}/ground current	I_{CC}		±75	mA
Power dissipation	P_D	(Note 1)	180	mW
Storage temperature	T_{stg}		-65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: 180 mW in the range of T_a = -40 to 85 °C. From T_a = 85 to 125 °C a derating factor of -3.25 mW/°C shall be applied until 50 mW.

10. Operating Ranges (Note)

Characteristics	Symbol	Test Condition	Rating	Unit
Supply voltage	V_{CC}		2.0 to 5.5	V
Input voltage	V_{IN}		0 to 5.5	V
Output voltage	V_{OUT}		0 to V_{CC}	V
Operating temperature	T_{opr}		-40 to 125	°C
Input rise and fall times	dt/dv	V_{CC} = 3.3 ± 0.3 V	0 to 100	ns/V
		V_{CC} = 5 ± 0.5 V	0 to 20	

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either V_{CC} or GND.

11. Electrical Characteristics

11.1. DC Characteristics (Unless otherwise specified, T_a = 25 °C)

Characteristics	Symbol	Test Condition		V_{CC} (V)	Min	Typ.	Max	Unit
High-level input voltage	V_{IH}	—		2.0	1.50	—	—	V
				3.0 to 5.5	V_{CC} × 0.7	—	—	
Low-level input voltage	V_{IL}	—		2.0	—	—	0.50	V
				3.0 to 5.5	—	—	V_{CC} × 0.3	
High-level output voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = -50 μA	2.0	1.9	2.0	—	V
				3.0	2.9	3.0	—	
				4.5	4.4	4.5	—	
			I_{OH} = -4 mA	3.0	2.58	—	—	
			I_{OH} = -8 mA	4.5	3.94	—	—	
Low-level output voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 μA	2.0	—	0.0	0.1	V
				3.0	—	0.0	0.1	
				4.5	—	0.0	0.1	
			I_{OL} = 4 mA	3.0	—	—	0.36	
			I_{OL} = 8 mA	4.5	—	—	0.36	
3-state output OFF-state leakage current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		5.5	—	—	±0.25	μA
Input leakage current	I_{IN}	V_{IN} = 5.5 V or GND		0 to 5.5	—	—	±0.1	μA
Quiescent supply current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	—	—	4.0	μA

11.2. DC Characteristics (Unless otherwise specified, T_a = -40 to 85 °C)

Characteristics	Symbol	Test Condition		V_{CC} (V)	Min	Max	Unit
High-level input voltage	V_{IH}	—		2.0	1.50	—	V
				3.0 to 5.5	V_{CC} × 0.7	—	
Low-level input voltage	V_{IL}	—		2.0	—	0.50	V
				3.0 to 5.5	—	V_{CC} × 0.3	
High-level output voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = -50 μA	2.0	1.9	—	V
				3.0	2.9	—	
				4.5	4.4	—	
			I_{OH} = -4 mA	3.0	2.48	—	
			I_{OH} = -8 mA	4.5	3.80	—	
Low-level output voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 μA	2.0	—	0.1	V
				3.0	—	0.1	
				4.5	—	0.1	
			I_{OL} = 4 mA	3.0	—	0.44	
			I_{OL} = 8 mA	4.5	—	0.44	
3-state output OFF-state leakage current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		5.5	—	±2.50	μA
Input leakage current	I_{IN}	V_{IN} = 5.5 V or GND		0 to 5.5	—	±1.0	μA
Quiescent supply current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	—	40.0	μA

11.3. DC Characteristics (Unless otherwise specified, T_a = -40 to 125 °C)

Characteristics	Symbol	Test Condition		V_{CC} (V)	Min	Max	Unit
High-level input voltage	V_{IH}	—		2.0	1.50	—	V
				3.0 to 5.5	V_{CC} × 0.7	—	
Low-level input voltage	V_{IL}	—		2.0	—	0.50	V
				3.0 to 5.5	—	V_{CC} × 0.3	
High-level output voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = -50 μA	2.0	1.9	—	V
				3.0	2.9	—	
				4.5	4.4	—	
			I_{OH} = -4 mA	3.0	2.40	—	
			I_{OH} = -8 mA	4.5	3.70	—	
Low-level output voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 μA	2.0	—	0.1	V
				3.0	—	0.1	
				4.5	—	0.1	
			I_{OL} = 4 mA	3.0	—	0.55	
			I_{OL} = 8 mA	4.5	—	0.55	
3-state output OFF-state leakage current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		5.5	—	±10.0	μA
Input leakage current	I_{IN}	V_{IN} = 5.5 V or GND		0 to 5.5	—	±2.0	μA
Quiescent supply current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	—	80.0	μA

11.4. AC Characteristics (Unless otherwise specified, T_a = 25 °C, Input: $t_r = t_f$ = 3 ns)

Characteristics	Part Number	Symbol	Note	Test Condition	V_{CC} (V)	C_L (pF)	Min	Typ.	Max	Unit
Propagation delay time	74VHC540FT	t_{PLH},t_{PHL}		—	3.3 ± 0.3	15	—	4.8	7.0	ns
						50	—	7.3	10.5	
					5.0 ± 0.5	15	—	3.7	5.0	
						50	—	5.2	7.0	
	74VHC541FT	t_{PLH},t_{PHL}		—	3.3 ± 0.3	15	—	5.0	7.0	ns
						50	—	7.5	10.5	
					5.0 ± 0.5	15	—	3.5	5.0	
						50	—	5.0	7.0	
3-state output enable time		t_{PZL},t_{PZH}		R_L = 1 kΩ	3.3 ± 0.3	15	—	6.8	10.5	ns
						50	—	9.3	14.0	
					5.0 ± 0.5	15	—	4.7	7.2	
						50	—	6.2	9.2	
3-state output disable time		t_{PLZ},t_{PHZ}		R_L = 1 kΩ	3.3 ± 0.3	50	—	11.2	15.4	ns
					5.0 ± 0.5	50	—	6.0	8.8	
Output skew		t_{osLH},t_{osHL}	(Note 1)	—	3.3 ± 0.3	50	—	—	1.5	ns
					5.0 ± 0.5	50	—	—	1.0	
Input capacitance		C_{IN}		—			—	4	10	pF
Output capacitance		C_{OUT}		—			—	6	—	pF
Power dissipation capacitance	74VHC540FT	C_{PD}	(Note 2)	—			—	17	—	pF
	74VHC541FT						—	18	—	

Note 1: Parameter guaranteed by design. (t_{osLH} = $|t_{PLH}m - t_{PLH}n|$, t_{osHL} = $|t_{PHL}m - t_{PHL}n|$)

Note 2: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation.

$I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/8$ (per bit)

11.5. AC Characteristics (Unless otherwise specified, T_a = -40 to 85 °C, Input: $t_r = t_f$ = 3 ns)

Characteristics	Part Number	Symbol	Note	Test Condition	V_{CC} (V)	C_L (pF)	Min	Max	Unit
Propagation delay time	74VHC540FT	t_{PLH},t_{PHL}		—	3.3 ± 0.3	15	1.0	8.5	ns
						50	1.0	12.0	
					5.0 ± 0.5	15	1.0	6.0	
						50	1.0	8.0	
	74VHC541FT	t_{PLH},t_{PHL}		—	3.3 ± 0.3	15	1.0	8.5	ns
						50	1.0	12.0	
					5.0 ± 0.5	15	1.0	6.0	
						50	1.0	8.0	
3-state output enable time		t_{PZL},t_{PZH}		R_L = 1 kΩ	3.3 ± 0.3	15	1.0	12.5	ns
						50	1.0	16.0	
					5.0 ± 0.5	15	1.0	8.5	
						50	1.0	10.5	
3-state output disable time		t_{PLZ},t_{PHZ}		R_L = 1 kΩ	3.3 ± 0.3	50	1.0	17.5	ns
					5.0 ± 0.5	50	1.0	10.0	
Output skew		t_{osLH},t_{osHL}	(Note 1)	—	3.3 ± 0.3	50	—	1.5	ns
					5.0 ± 0.5	50	—	1.0	
Input capacitance		C_{IN}		—			—	10	pF

Note 1: Parameter guaranteed by design. (t_{osLH} = $|t_{PLH}m - t_{PLH}n|$, t_{osHL} = $|t_{PHL}m - t_{PHL}n|$)

11.6. AC Characteristics (Unless otherwise specified, T_a = -40 to 125 °C, Input: $t_r = t_f$ = 3 ns)

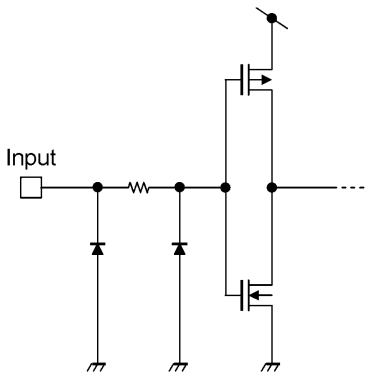
Characteristics	Part Number	Symbol	Note	Test Condition	V_{CC} (V)	C_L (pF)	Min	Max	Unit
Propagation delay time	74VHC540FT	t_{PLH},t_{PHL}		—	3.3 ± 0.3	15	1.0	10.0	ns
						50	1.0	13.5	
					5.0 ± 0.5	15	1.0	7.0	
						50	1.0	9.0	
Propagation delay time	74VHC541FT	t_{PLH},t_{PHL}		—	3.3 ± 0.3	15	1.0	10.0	ns
						50	1.0	13.5	
					5.0 ± 0.5	15	1.0	7.0	
						50	1.0	9.0	
3-state output enable time		t_{PZL},t_{PZH}		R_L = 1 kΩ	3.3 ± 0.3	15	1.0	14.0	ns
						50	1.0	17.5	
					5.0 ± 0.5	15	1.0	9.5	
						50	1.0	11.5	
3-state output disable time		t_{PLZ},t_{PHZ}		R_L = 1 kΩ	3.3 ± 0.3	50	1.0	19.5	ns
					5.0 ± 0.5	50	1.0	11.0	
Output skew		t_{osLH},t_{osHL}	(Note 1)	—	3.3 ± 0.3	50	—	1.5	ns
					5.0 ± 0.5	50	—	1.0	
Input capacitance		C_{IN}		—			—	10	pF

Note 1: Parameter guaranteed by design. ($t_{osLH} = |t_{PLH}m - t_{PLH}n|$, $t_{osHL} = |t_{PHL}m - t_{PHL}n|$)

11.7. Noise Characteristics (Unless otherwise specified, T_a = 25 °C, Input: $t_r = t_f$ = 3 ns)

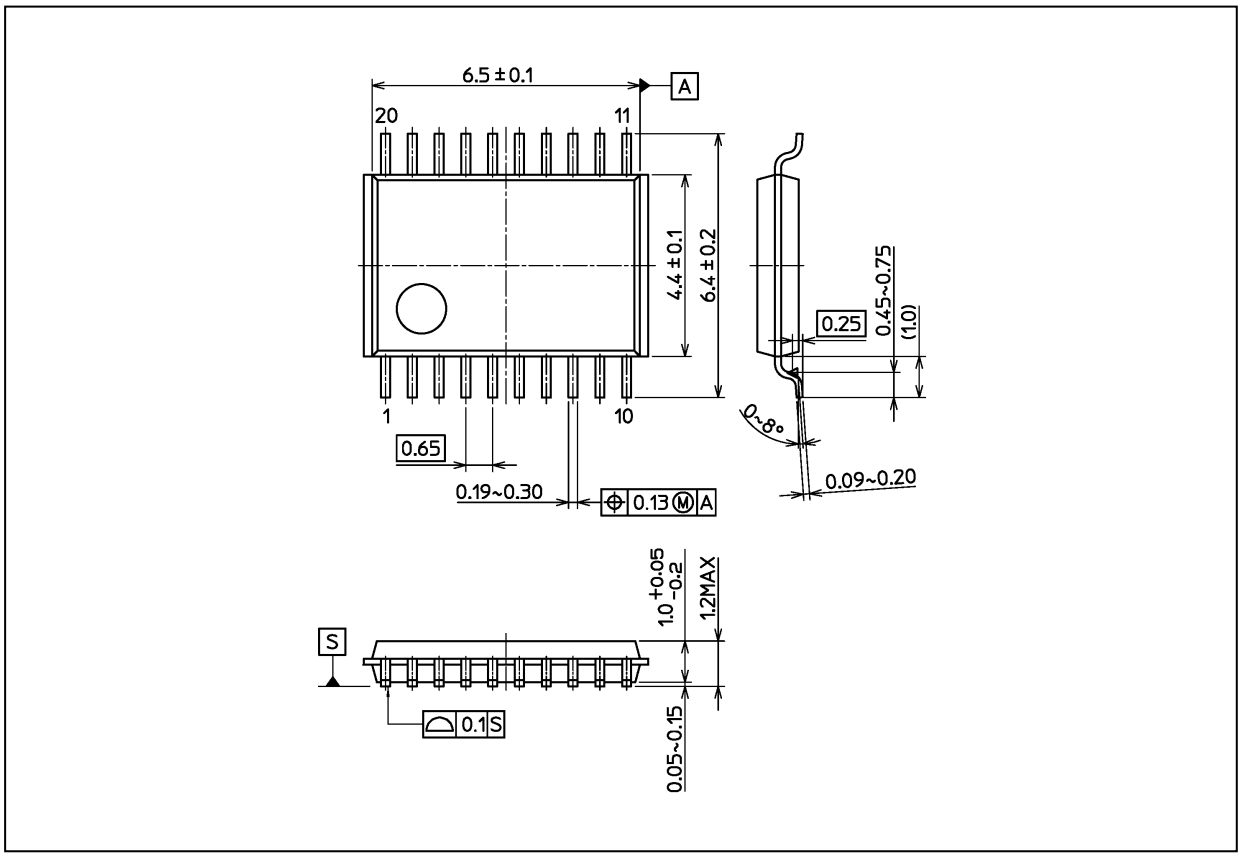
Characteristics	Symbol	Test Condition	V_{CC} (V)	Typ.	Limit	Unit
Quiet output maximum dynamic V_{OL}	V_{OLP}	C_L = 50 pF	5.0	0.7	1.0	V
Quiet output minimum dynamic V_{OL}	V_{OLV}	C_L = 50 pF	5.0	-0.7	-1.0	V
Minimum high-level dynamic input voltage	V_{IHD}	C_L = 50 pF	5.0	—	3.5	V
Maximum low-level dynamic input voltage	V_{ILD}	C_L = 50 pF	5.0	—	1.5	V

12. Internal Equivalent Circuit



Package Dimensions

Unit: mm



Weight: 0.071 g (typ.)

Package Name(s)
Nickname: TSSOP20B

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