

## Configurable Four Output, Low Jitter Crystal-less™ Clock Generator

### Features

- Low RMS Phase Jitter: <1 ps (typ.)
- High Stability:  $\pm 25$  ppm,  $\pm 50$  ppm
- Wide Temperature Range:
  - Industrial  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$
  - Ext. Commercial  $-20^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$
- High Supply Noise Rejection:  $-50$  dBc
- Four Format-Configurable Outputs:
  - LVPECL, LVDS, HCSL, LVCMOS
- Available Pin-Selectable Frequency Table
  - 1 Pin per Bank for 2 Frequency Sets
- Wide Frequency Range:
  - 2.3 MHz – 460 MHz
- 20-Pin QFN Footprint (5.0 mm x 3.2 mm)
- Excellent Shock and Vibration Immunity
- High Reliability
  - 20x better MTF than quartz-based devices
- Wide Supply Range of 2.25V to 3.6V
- Lead Free and RoHS-Compliant
- AEC-Q100 Automotive Qualified

### Applications

- Communications and Networks
- Ethernet
  - 1G, 10GBASE-T/KR/LR/SR, and FCoE
- Storage Area Networks
  - SATA, SAS, Fibre Channel
- Passive Optical Networks
  - EPON, 10G-EPON, GPON, 10G-PON
- HD/SD/SDI Video and Surveillance
- Automotive
- Media and Video
- Embedded and Industrial

### General Description

The DSC400 is a four output crystal-less™ clock generator. It utilizes proven PureSilicon™ MEMS technology to provide excellent jitter and stability while incorporating additional device functionality.

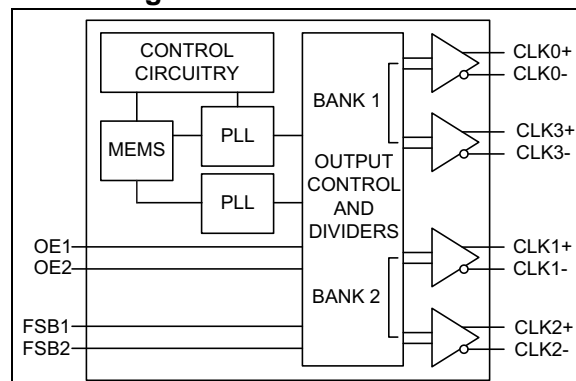
The nominal frequencies of the outputs can be identical or independently derived from common PLLs.

Each output may be configured independently to support a single-ended LVCMOS interface or a differential interface. Differential options include LVPECL, LVDS, or HCSL.

The DSC400 provides two independent select lines for choosing between two sets of pre-configured frequencies per bank. It also has two OE pins to allow for enabling and disabling outputs.

The DSC400 is packaged in a 20-pin QFN (5 mm x 3.2 mm) and is available in extended commercial and industrial temperature grades.

### Block Diagram



# DSC400

## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings †

Supply Voltage .....	-0.3V to +4.0V
Input Voltage .....	-0.3V to $V_{DD}+0.3V$
ESD Protection (HBM) .....	.4 kV
ESD Protection (MM) .....	400V
ESD Protection (CDM) .....	1.5 kV

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

### ELECTRICAL CHARACTERISTICS

Specifications:  $V_{DD} = 3.3V$ ;  $T_A = +25^\circ C$  unless otherwise specified.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Supply Voltage (Note 1)	$V_{DD}$	2.25	—	3.6	V	—
Core Supply Current (Note 2)	$I_{DDCORE}$	—	40	44	mA	OE(1:2) = 0. All outputs disabled.
Frequency Stability	$\Delta f$	—	—	$\pm 25$	ppm	All temperature and $V_{DD}$ ranges.
		—	—	$\pm 50$		
Aging - First Year	$\Delta f_{Y1}$	—	—	$\pm 5$	ppm	One year at $+25^\circ C$
Aging - After First Year	$\Delta f_{Y2+}$	—	—	$< \pm 1$	ppm/yr	Year two and beyond at $+25^\circ C$
Start-up Time (Note 3)	$t_{SU}$	—	—	5	ms	$T = +25^\circ C$
Input Logic Levels	$V_{IH}$	$0.75 \times V_{DD}$	—	—	V	Input logic high
	$V_{IL}$	—	—	$0.25 \times V_{DD}$		Input logic low
Output Disable Time (Note 4)	$t_{DA}$	—	—	5	ns	OE(1:2) transition from 1 to 0
Output Enable Time (Note 4)	$t_{EN}$	—	—	20	ns	OE(1:2) transition from 0 to 1
Pull-Up Resistor	$R_{PU}$	—	40	—	k $\Omega$	All input pins have an internal pull-up

- Note 1:**  $V_{DD}$  pins should be filtered with a 0.1  $\mu F$  capacitor connected between  $V_{DD}$  and  $V_{SS}$ .  
**Note 2:** The addition of  $I_{DDCORE}$  and  $I_{DDIO}$  provides the total current consumption of the device.  
**Note 3:**  $t_{SU}$  is time to 100 ppm stable output frequency after  $V_{DD}$  is applied and outputs are enabled.  
**Note 4:** See the [Output Waveform](#) section for more information.

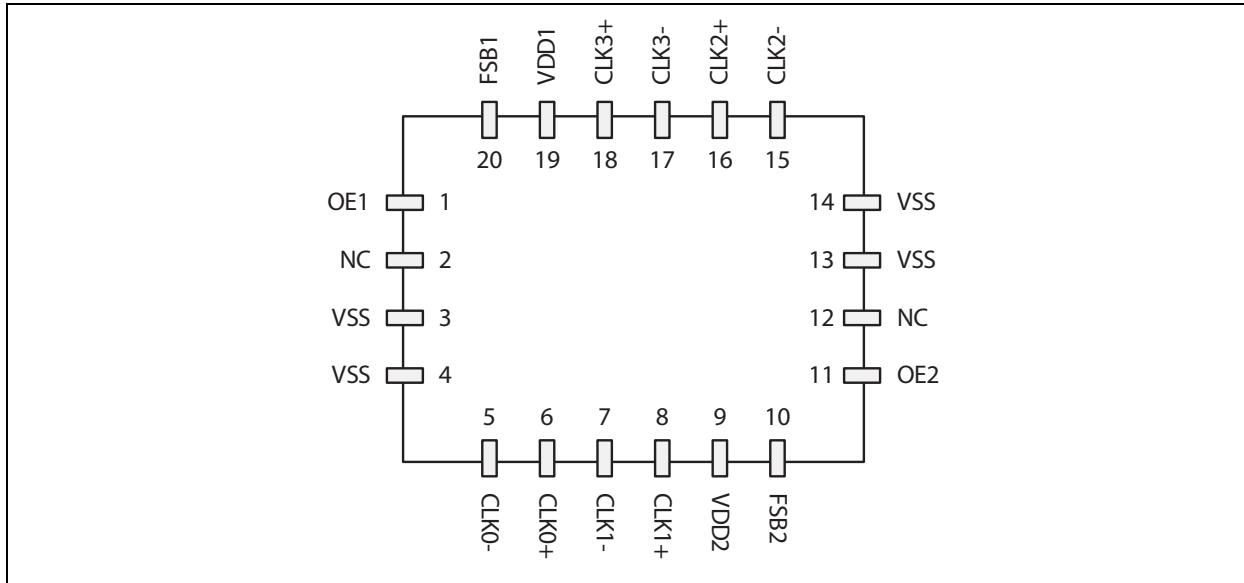
## TEMPERATURE SPECIFICATIONS (Note 1)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
<b>Temperature Ranges</b>						
Operating Temperature Range (T)	T <sub>A</sub>	-20	—	+70	°C	Ordering Option E
	T <sub>A</sub>	-40	—	+85	°C	Ordering Option I
Junction Temperature	T <sub>J</sub>	—	—	+150	°C	—
Storage Temperature Range	T <sub>S</sub>	-40	—	+150	°C	—
Soldering Temperature	—	—	—	+260	°C	40 sec. max.

**Note 1:** The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature, and the thermal resistance from junction to air (i.e., T<sub>A</sub>, T<sub>J</sub>, θ<sub>JA</sub>). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +125°C rating. Sustained junction temperatures above +125°C can impact the device reliability.

# DSC400

## 2.0 PIN DESCRIPTIONS



**FIGURE 2-1:** Pin Configuration, 20-Pin QFN (5.0 mm x 3.2 mm)

The descriptions of the pins are listed in [Table 2-1](#).

**TABLE 2-1: PIN FUNCTION TABLE**

Pin Number	Pin Name	Pin Type	Description
1	OE1	I	Output Enable for Bank1 (CLK0 and CLK3); Active-High. See <a href="#">Table 3-1</a> .
2	NC	N/A	Leave unconnected or connect to ground.
3	V <sub>SS</sub>	PWR	Ground.
4	V <sub>SS</sub>	PWR	Ground.
5	CLK0-	O	Complement output of differential pair 0 (off when in LVCMOS format).
6	CLK0+	O	True output of differential pair 0 or LVCMOS output 0.
7	CLK1-	O	Complement output of differential pair 1 (off when in LVCMOS format).
8	CLK1+	O	True output of differential pair 1 or LVCMOS output 1.
9	V <sub>DD2</sub>	PWR	Power Supply for Bank2 (CLK1 and CLK2).
10	FSB2	I	Input for selecting pre-configured frequencies on Bank2 (CLK1 and CLK2).
11	OE2	I	Output Enable for Bank2 (CLK1 and CLK2); Active-High. See <a href="#">Table 3-1</a> .
12	NC	N/A	Leave unconnected or connect to ground.
13	V <sub>SS</sub>	PWR	Ground.
14	V <sub>SS</sub>	PWR	Ground.
15	CLK2-	O	Complement output of differential pair 2 (off when in LVCMOS format).
16	CLK2+	O	True output of differential pair 2 or LVCMOS output 2.
17	CLK3-	O	Complement output of differential pair 3 (off when in LVCMOS format).
18	CLK3+	O	True output of differential pair 3 or LVCMOS output 3.
19	V <sub>DD1</sub>	PWR	Power Supply for Bank1 (CLK0 and CLK3).
20	FSB1	I	Input for selecting pre-configured frequencies on Bank1 (CLK0 and CLK3).

## 3.0 OPERATIONAL DESCRIPTION

The DSC400 is a crystal-less™ clock generator. Unlike older clock generators in the industry, it does not require an external crystal to operate; it relies on the integrated MEMS resonator that interfaces with internal PLLs. This technology enhances performance and reliability by allowing tighter frequency stability over a far wider temperature range. In addition, the higher resistance to shock and vibration decreases the aging rate to allow for much improved product life in the system.

### 3.1 Inputs

There are four input signals in the device. Each has an internal (40 kΩ) pull-up to default the selection to a high (1). Inputs can be controlled through hardware strapping method with a resistor to ground to assert the input low (0). Inputs may also be controlled by other components' GPIOs

In case more than one frequency set is desired, FSB1 and FSB2 are used to independently select one of two sets per bank. FSB1 selects the pre-configured set on Bank1 (CLK0 and CLK3) and FSB2 selects the pre-configured set on Bank2 (CLK1 and CLK2), as shown in [Table 1-1](#) in the [Product Identification System](#) section.

If there is a requirement to disable outputs, the inputs OE1 and OE2 are used in conjunction to disable the banks of outputs. Outputs are disabled in tri-state (Hi-Z) mode. See [Table 3-1](#) for more information.

**TABLE 3-1: OUTPUT ENABLE SELECTION TABLE**

OE1	OE2	Bank 1 (CLK0 & CLK3)	Bank 2 (CLK1 & CLK2)
0	0	Hi-Z	Hi-Z
0	1	Hi-Z	Running
1	0	Running	Hi-Z
1	1	Running	Running

### 3.2 Outputs

The four outputs are grouped into two banks. Each bank is supplied by an independent  $V_{DD}$  to allow for optimized noise isolation between the two banks. Each bank provides two synchronous outputs generated by a common PLL:

- Bank1 is composed of outputs CLK0 and CLK3.
- Bank2 is composed of outputs CLK1 and CLK2.

Each output may be pre-configured independently to be one of the following formats: LVCMOS, LVDS, LVPECL or HCSL. In case the output is configured to be single-ended LVCMOS, the frequency is generated on the true output (CLKx+) and the complement output (CLKx-) is shut off in a low state. Frequencies can be

chosen from 2.3 MHz to 460 MHz for differential outputs and from 2.3 MHz to 170 MHz on LVCMOS outputs.

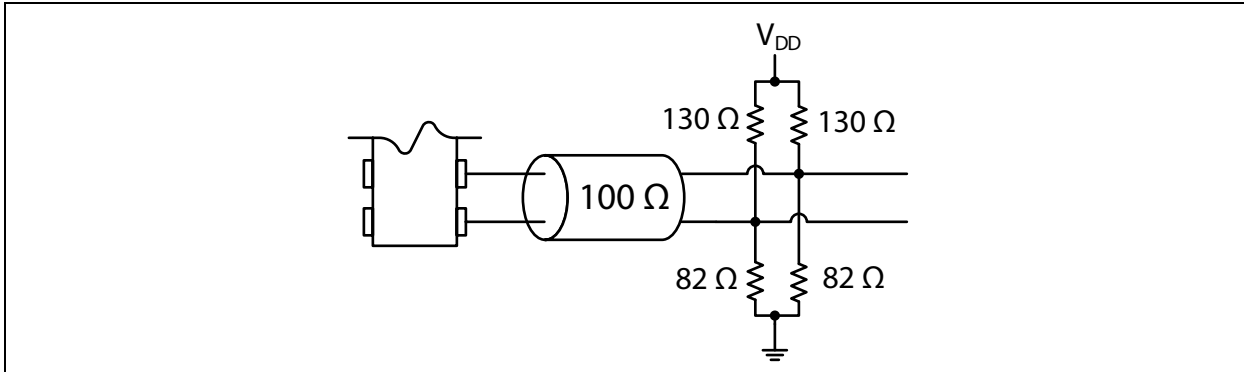
### 3.3 Power

$V_{DD1}$  and  $V_{DD2}$  supply the power to banks 1 and 2 respectively. Each  $V_{DD}$  may each have a different supply voltage from the other as long as it is within the 2.25V to 3.6V range. Each  $V_{DD}$  pin should have a 0.1 μF capacitor to filter high-frequency noise.  $V_{SS}$  is common to the entire device.

# DSC400

## 4.0 TERMINATION SCHEMES

### 4.1 LVPECL



**FIGURE 4-1:** Typical LVPECL Termination Scheme.

**TABLE 4-1: LVPECL OUTPUTS (Note 1)**

Parameter	Symbol	Min.	Typ.	Max.	Units	Condition
Output Logic Levels	V <sub>OH</sub>	V <sub>DD</sub> - 1.08	—	—	V	Output Logic High, R <sub>L</sub> = 50Ω to V <sub>DD</sub> -2V
	V <sub>OL</sub>	—	—	V <sub>DD</sub> - 1.55		Output Logic Low, R <sub>L</sub> = 50Ω to V <sub>DD</sub> -2V
Peak-to-Peak Output Swing	—	—	800	—	mV	Single-Ended
Output Transition Time (Note 2)	t <sub>R</sub>	—	250	—	ps	Rise Time. 20% to 80%; R <sub>L</sub> = 50Ω to V <sub>DD</sub> -2V
	t <sub>F</sub>	—	250	—		Fall Time. 20% to 80%; R <sub>L</sub> = 50Ω to V <sub>DD</sub> -2V
Frequency	f <sub>0</sub>	2.3	—	460	MHz	Single Frequency
Output Duty Cycle	SYM	48	—	52	%	Differential
IO Supply Current (Note 3)	I <sub>DDIO</sub>	—	35	38	mA	Per Output at 125 MHz
Period Jitter (Note 4)	J <sub>PER</sub>	—	2.5	—	ps <sub>RMS</sub>	CLK(0:3) = 156.25 MHz
Integrated Phase Noise	J <sub>PH</sub>	—	0.25	—	ps <sub>RMS</sub>	200 kHz to 20 MHz @ 156.25 MHz
		—	0.38	—		100 kHz to 20 MHz @ 156.25 MHz
		—	1.7	2		12 kHz to 20 MHz @ 156.25 MHz

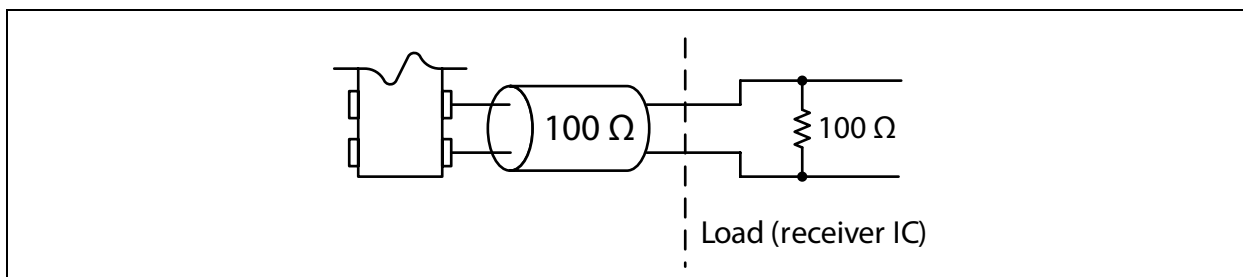
**Note 1:** LVPECL applicable to extended commercial temperature only.

**2:** See the [Output Waveform](#) section for more information.

**3:** The addition of I<sub>DDCORE</sub> and I<sub>DDIO</sub> provides the total current consumption of the device.

**4:** Period jitter includes crosstalk from adjacent output.

## 4.2 LVDS



**FIGURE 4-2:** Typical LVDS Termination Scheme.

If the 100Ω clamping resistor does not exist inside the receiving device, it should be added externally on the PCB and placed as close as possible to the receiver.

**TABLE 4-2: LVDS OUTPUTS**

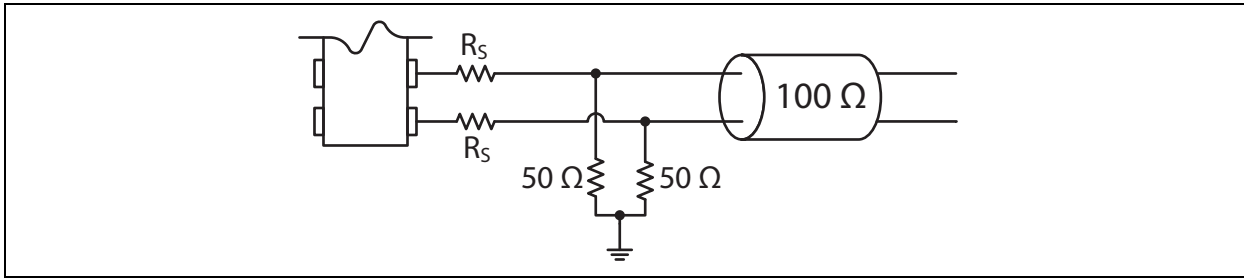
Parameter	Symbol	Min.	Typ.	Max.	Units	Condition
Output Offset Voltage	$V_{OS}$	1.125	—	1.4	V	R = 100Ω Differential
Delta Offset Voltage	$\Delta V_{OS}$	—	—	50	mV	—
Peak-to-Peak Output Swing	$V_{PP}$	—	350	—	mV	Single-Ended
Output Transition Time (Note 1)	$t_R$	—	200	—	ps	Rise Time, 20% to 80%, $R_L = 50\Omega$ , $C_L = 2\text{ pF}$
	$t_F$	—	200	—		Fall Time, 20% to 80%, $R_L = 50\Omega$ , $C_L = 2\text{ pF}$
Frequency	$f_0$	2.3	—	460	MHz	Single Frequency
Output Duty Cycle	SYM	48	—	52	%	Differential
IO Supply Current (Note 2)	$I_{DDIO}$	—	9	12	mA	Per Output at 125 MHz.
Period Jitter	$J_{PER}$	—	2.5	—	$ps_{RMS}$	—
Integrated Phase Noise	$J_{PH}$	—	0.28	—	$ps_{RMS}$	200 kHz to 20 MHz @ 156.25 MHz
		—	0.4	—		100 kHz to 20 MHz @ 156.25 MHz
		—	1.7	2.0		12 kHz to 20 MHz @ 156.25 MHz

**Note 1:** See the [Output Waveform](#) section for more information.

**2:** The addition of  $I_{DDCORE}$  and  $I_{DDIO}$  provides the total current consumption of the device.

# DSC400

## 4.3 HCSL



**FIGURE 4-3:** Typical HCSL Termination Scheme.

$R_S$  is a series resistor implemented to match the trace impedance. Depending on the board layout, the value may range from 0 $\Omega$  to 30 $\Omega$ .

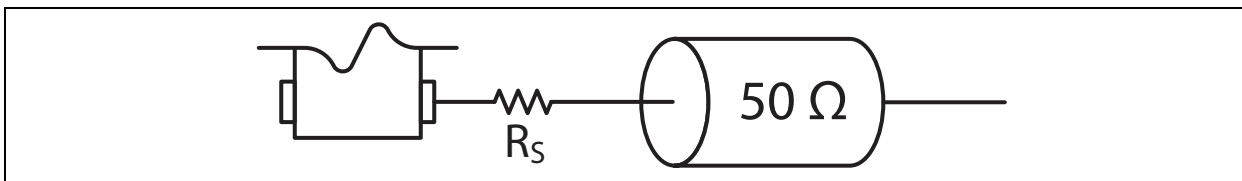
**TABLE 4-3: HCSL OUTPUTS**

Parameter	Symbol	Min.	Typ.	Max.	Units	Condition
Output Logic Levels	$V_{OH}$	0.725	—	—	V	Output Logic High, $R_L = 50\Omega$
	$V_{OL}$	—	—	0.1		Output Logic Low, $R_L = 50\Omega$
Peak-to-Peak Output Swing	—	—	750	—	mV	Single-Ended
Output Transition Time (Note 1)	$t_R$	200	—	400	ps	Rise Time, 20% to 80%, $R_L = 50\Omega$ , $C_L = 2$ pF
	$t_F$	200	—	400		Fall Time, 20% to 80%, $R_L = 50\Omega$ , $C_L = 2$ pF
Frequency	$f_0$	2.3	—	460	MHz	Single Frequency
Output Duty Cycle	SYM	48	—	52	%	Differential
IO Supply Current (Note 2)	$I_{DDIO}$	—	20	22	mA	Per Output at 125 MHz.
Period Jitter	$J_{PER}$	—	2.5	—	ps <sub>RMS</sub>	—
Integrated Phase Noise	$J_{PH}$	—	0.25	—	ps <sub>RMS</sub>	200 kHz to 20 MHz @ 156.25 MHz
		—	0.37	—		100 kHz to 20 MHz @ 156.25 MHz
		—	1.7	2.0		12 kHz to 20 MHz @ 156.25 MHz

**Note 1:** See the [Output Waveform](#) section for more information.

**2:** The addition of  $I_{DDCORE}$  and  $I_{DDIO}$  provides the total current consumption of the device.

## 4.4 LVCMOS



**FIGURE 4-4:** Typical LVCMOS Termination Scheme.

$R_S$  is a series resistor implemented to match the trace impedance to that of the clock output. Depending on the board layout, the value may range from 0 $\Omega$  to 27 $\Omega$ .

**TABLE 4-4: LVCMOS OUTPUTS**

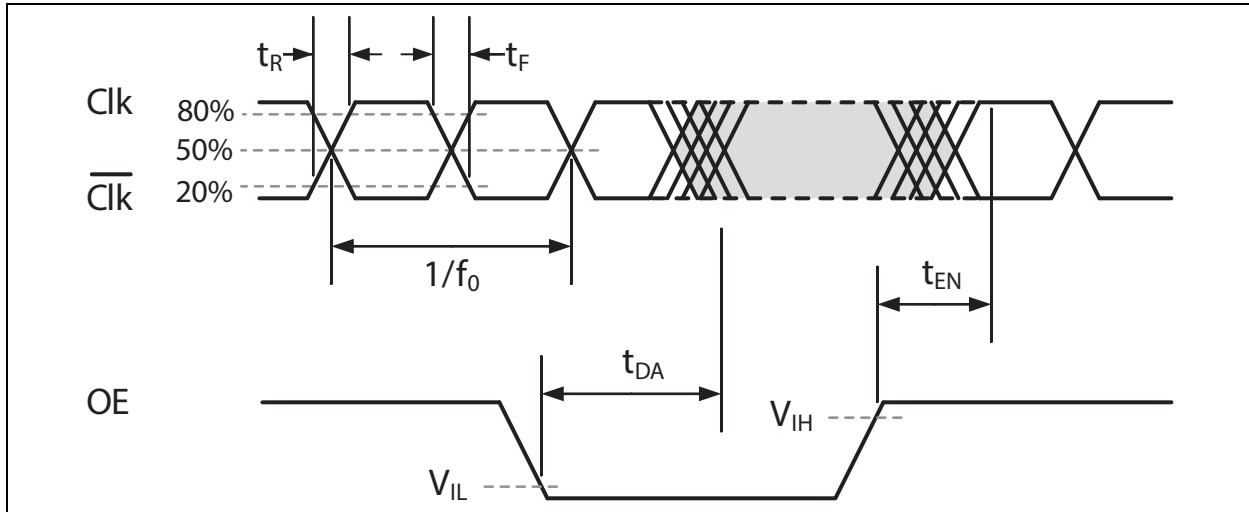
Parameter	Symbol	Min.	Typ.	Max.	Units	Condition
Output Logic Levels	$V_{OH}$	$0.9 \times V_{DD}$	—	—	V	Output Logic High, $I = \pm 6$ mA
	$V_{OL}$	—	—	$0.1 \times V_{DD}$		Output Logic Low, $I = \pm 6$ mA
Output Transition Time (Note 1)	$t_R$	—	1.1	2.0	ns	Rise Time, 20% to 80%, $C_L = 15$ pF
	$t_F$	—	1.3	2.0		Fall Time, 20% to 80%, $C_L = 15$ pF
Frequency	$f_0$	2.3	—	170	MHz	All Temperature Ranges, Except Automotive
		—	—	100		Automotive Temperature Range
Output Duty Cycle	SYM	44	—	55	%	—
IO Supply Current (Note 2)	$I_{DDIO}$	—	11	14	mA	Per Output at 125 MHz, $C_L = 15$ pF
Period Jitter	$J_{PER}$	—	3	—	ps <sub>RMS</sub>	CLK(0:3) = 125 MHz
Integrated Phase Noise	$J_{PH}$	—	0.3	—	ps <sub>RMS</sub>	200 kHz to 20 MHz @ 125 MHz
		—	0.38	—		100 kHz to 20 MHz @ 125 MHz
		—	1.7	2.0		12 kHz to 20 MHz @ 125 MHz

**Note 1:** See the [Output Waveform](#) section for more information.

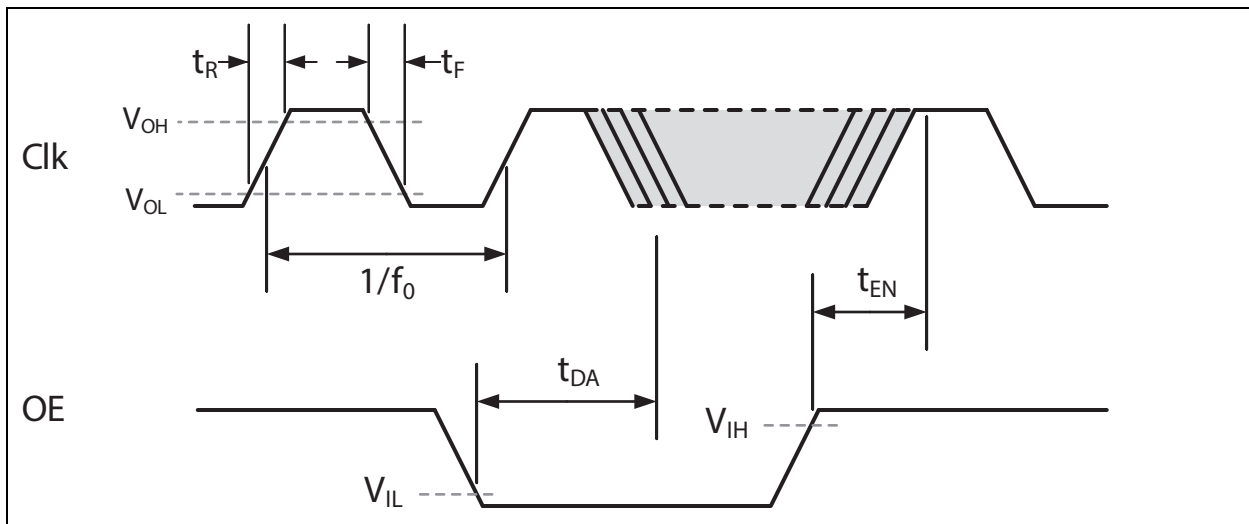
**2:** The addition of  $I_{DDCORE}$  and  $I_{DDIO}$  provides the total current consumption of the device.

# DSC400

## 5.0 OUTPUT WAVEFORM



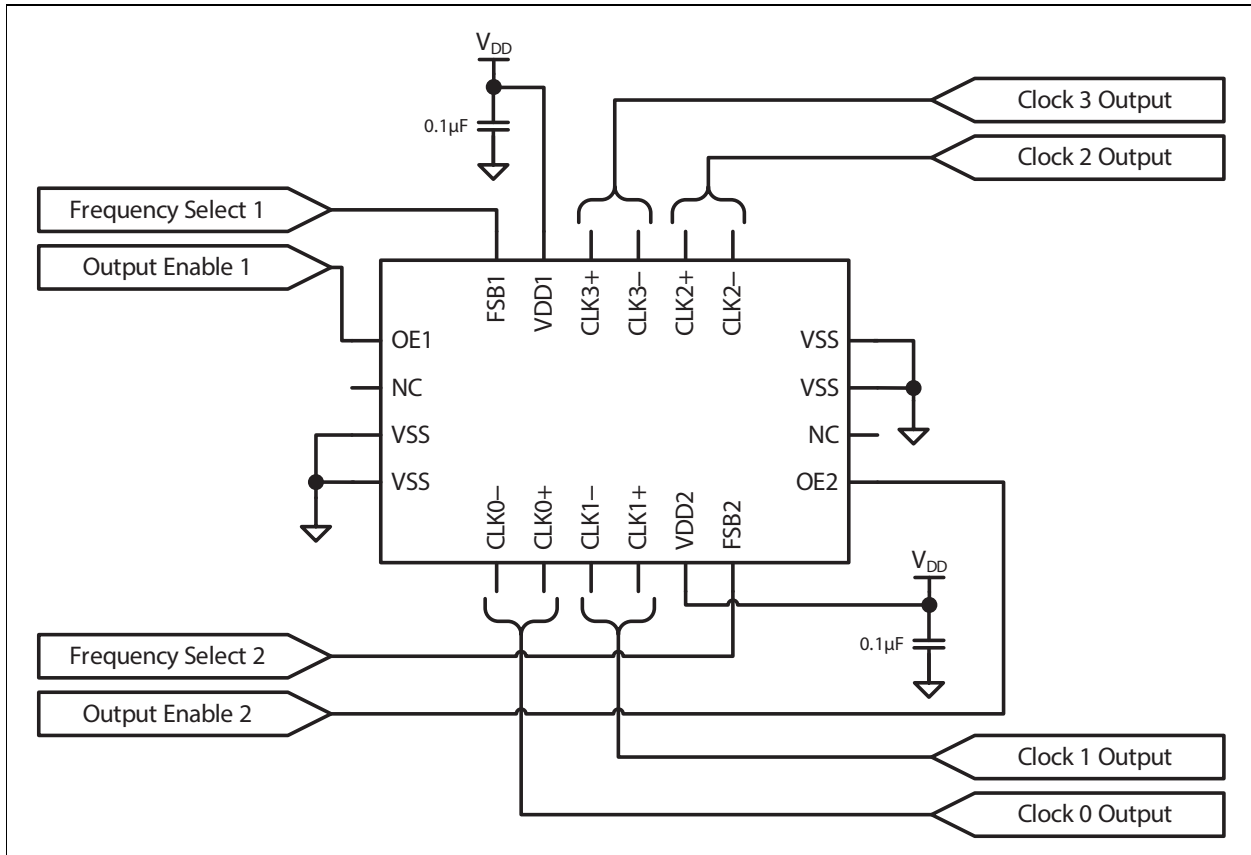
**FIGURE 5-1:** Differential Output (LVDS, LVPECL, HCSL).



**FIGURE 5-2:** LVCMOS Output.

## 6.0 CONNECTION DIAGRAM

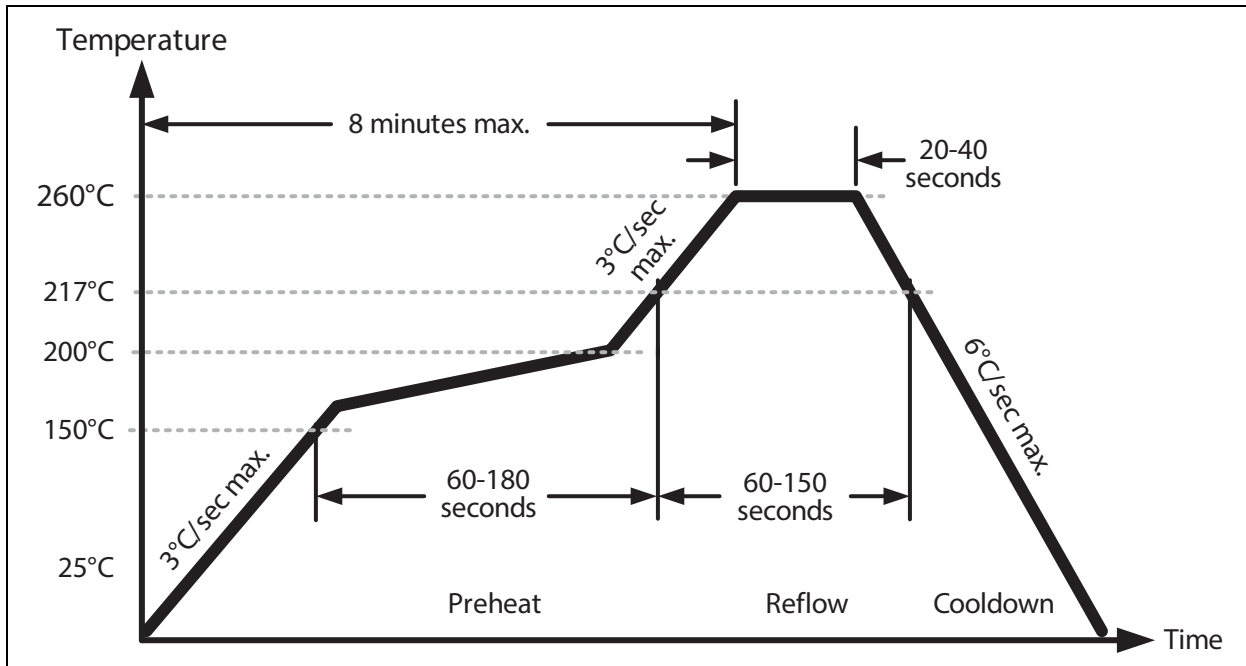
The connection diagram below includes recommended capacitors to be placed on each  $V_{DD}$  for noise filtering.



**FIGURE 6-1:** DSC400 Connection Diagram.

# DSC400

## 7.0 SOLDER REFLOW PROFILE



MSL 1 @ 260°C refer to JSTD-020C	
Ramp-Up Rate (200°C to Peak Temp)	3°C/sec. max.
Preheat Time 150°C to 200°C	60-180 sec.
Time Maintained above 217°C	60-150 sec.
Peak Temperature	255°C to 260°C
Time within 5°C of Actual Peak	20-40 sec.
Ramp-Down Rate	6°C/sec. max.
Time 25°C to Peak Temperature	8 minutes max.

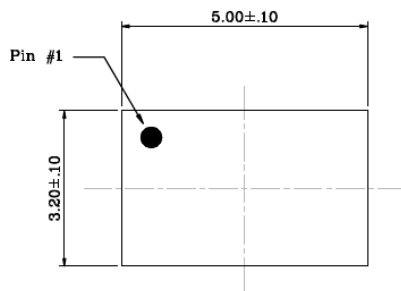
## 8.0 PACKAGE MARKING INFORMATION

### 20-Lead QFN 5.0 mm x 3.2 mm Package Outline and Recommended Land Pattern

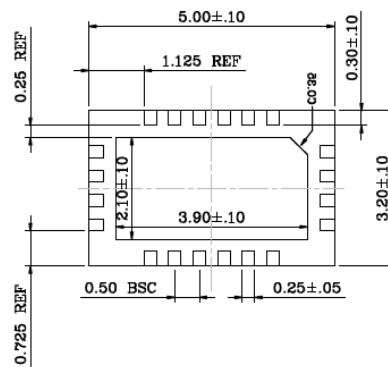
**TITLE**

20 LEAD QFN 5.0x3.2mm PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

DRAWING #	UNIT	MM
QFN5032-20LD-PL-1		



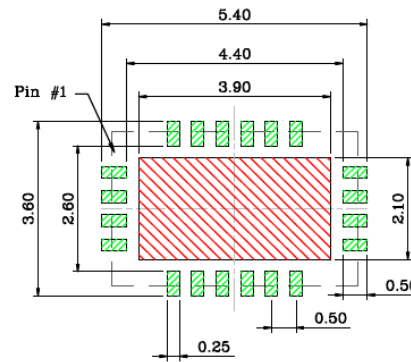
Top View



Bottom View



Side View



Recommended Land Pattern

**NOTE:**

1. Green shaded rectangles in Recommended Land Pattern are solder stencil opening.
2. Red shaded rectangle in Recommended Land Pattern is keep-out area.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>.

# DSC400

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NOTES:

## APPENDIX A: REVISION HISTORY

### Revision A (September 2016)

- Converted Micrel data sheet DSC400 to Microchip DS20005612A.
- Minor text changes throughout.

# DSC400

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NOTES:

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	X	X	X	X	Qxxxx	X	X	X	X
Device	CLK3 Output Format	CLK2 Output Format	CLK1 Output Format	CLK0 Output Format	Freq. Code	Package	Temp. Range	Stability	Packing
<b>Device:</b>	DSC400: Configurable Four Output, Low Jitter Crystal-less Clock Generator								
<b>CLK3 Output Format:</b>	0	=	OFF						
	1	=	LVC MOS						
	2	=	LVPECL						
	3	=	LVDS						
	4	=	HCSL						
<b>CLK2 Output Format:</b>	1	=	LVC MOS						
	2	=	LVPECL						
	3	=	LVDS						
	4	=	HCSL						
<b>CLK1 Output Format:</b>	0	=	OFF						
	1	=	LVC MOS						
	2	=	LVPECL						
	3	=	LVDS						
	4	=	HCSL						
<b>CLK0 Output Format:</b>	1	=	LVC MOS						
	2	=	LVPECL						
	3	=	LVDS						
	4	=	HCSL						
<b>Frequency Code:</b>	Qxxxx	=	This code is assigned by the factory. See the table in this section for more information.						
<b>Package:</b>	K	=	20-Pin QFN						
<b>Temperature Range:</b>	E	=	-20°C to +70°C						
	I	=	-40°C to +85°C						
<b>Stability:</b>	1	=	±50 ppm						
	2	=	±25 ppm						
<b>Packing:</b>	T	=	Tape & Reel						

<b>Examples:</b>
a) DSC400-2143QxxxxKE1T: Configurable Four Output, Low Jitter Crystal-less Clock Generator; LVPECL CLK3; LVC MOS CLK2; HCSL CLK1; LVDS CLK0; Frequency Code; 20-Pin QFN; -20°C to +70°C Temp. Range; ±50 ppm Stability; Tape & Reel
b) DSC400-4132QxxxxKI2T: Configurable Four Output, Low Jitter Crystal-less Clock Generator; HCSL CLK3; LVC MOS CLK2; LVDS CLK1; LVPECL CLK0; Frequency Code; 20-Pin QFN; -40°C to +85°C Temp. Range; ±25 ppm Stability; Tape & Reel
c) DSC400-0202QxxxxKE2T: Configurable Four Output, Low Jitter Crystal-less Clock Generator; OFF CLK3; LVPECL CLK2; OFF CLK1; LVPECL CLK0; Frequency Code; 20-Pin QFN; -20°C to +70°C Temp. Range; ±25 ppm Stability; Tape & Reel
d) DSC400-1111QxxxxKI1T: Configurable Four Output, Low Jitter Crystal-less Clock Generator; LVC MOS CLK3 through CLK0; Frequency Code; 20-Pin QFN; -40°C to +85°C Temp. Range; ±50 ppm Stability; Tape & Reel

### 1.0 FACTORY CONFIGURATION CODE ASSIGNMENT OF QXXXX

The DSC400 is meant for customers to define their own frequency requirements at the four available outputs. The Qxxxx number identifies these specific customer requirements and is assigned by the factory.

**TABLE 1-1: EXAMPLE OF HOW FSB1 & FSB2 ARE APPLIED & THE QXXXX ASSIGNMENT**

Bank1	Outputs	FSB1		Qxxxx Number
		1 (default)	0	
	CLK0	125 MHz	150 MHz	
	CLK3	50 MHz	25 MHz	
Bank2	Outputs	FSB2		
		1 (default)	0	
		CLK1	156.25 MHz	100 MHz
	CLK2	156.25 MHz	100 MHz	

# DSC400

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NOTES:

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**Note the following details of the code protection feature on Microchip devices:**

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
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