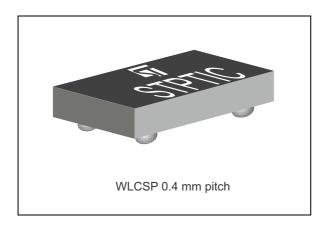
STPTIC-56G2



Parascan™ tunable integrated capacitor

Datasheet - production data



Features

- High power capability
- 5:1 tuning range
- High linearity
- High quality factor (Q)
- Low leakage current
- Compatible with high voltage control IC (STHVDAC series)
- · Available in wafer level chip scale package:
 - WLCSP package 0.59 x 0.71 x 0.3 mm
- ECOPACK®2 compliant component

Benefit

 RF tunable passive implementation in mobile phones to optimize antenna radiated performance

Applications

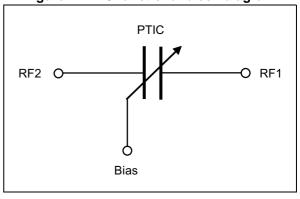
- Cellular antenna open loop tunable matching network in multi-band GSM/WCDMA/LTE mobile phone
- · Open loop tunable RF filters

Description

The ST integrated tunable capacitor offers excellent RF performance, low power consumption and high linearity required in adaptive RF tuning applications. The fundamental building block of PTIC is a tunable material called Parascan™, which is a version of barium strontium titanate (BST) developed by Paratek Microwave.

BST capacitors are tunable capacitors intended for use in mobile phone application and dedicated to RF tunable applications. These tunable capacitors are controlled through an extended bias voltage ranging from 1 to 24 V. The implementation of BST tunable capacitor in mobile phones enables significant improvement in terms of radiated performance making the performance almost insensitive to the external environment.

Figure 1. PTIC functional block diagram



TM: Parascan is a trademark of Paratek Microwave Inc.

Electrical characteristics STPTIC-56G2

1 Electrical characteristics

Table 1. Absolute maximum ratings (limiting values)

Symbol	Parameter	Rating	Unit
P _{IN}	Input peak power RF _{IN} (CW mode)/all RF ports	+40	dBm
V _{ESD(HBM)}	Human body model, JESD22-A114-B, all I/O	Class 1B ⁽¹⁾	V
V _{ESD(MM)}	Machine model, JESD22-A115-A, all I/O	100	V
T _{device}	Device temperature	+125	°C
T _{stg}	Storage temperature	-55 to +150	C
V _x	Bias voltage	25	V

^{1.} Class 1B defined as passing 500 V, but fails after exposure to 1000V ESD pulse.

Table 2. Recommended operating conditions

Symbol	Parameter		Rating		Unit
	Farameter	Min.	Тур.	Max.	dBm MHz
P_{IN}	RF input power		+33		dBm
F _{OP}	Operating frequency	700		2700	MHz
T _{device}	Device temperature			+100	°C
T _{OP}	Operating temperature	-30		+85	
V _{BIAS}	Bias voltage	1		24	V

Table 3. Representative performance (T_{amb} = 25 °C otherwise specified)

Complete	Danamatan	Candidana		Value	!	pF pF nA dBm
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
C _{1V}	capacitor at 1 V bias	STPTIC-56G2	5.72	6.5	7.28	pF
C _{2V}	capacitor at 2 V bias	STPTIC-56G2		5.6		pF
C _{24V}	capacitor at 24 V bias	STPTIC-56G2	1.03	1.12	1.21	pF
ΔC	Tuning range	Ratio between C _{1V} /C _{24V} ⁽¹⁾	5/1			
ΙL	Leakage current	Measured with V _{bias} = 24 V			100	nA
Q _{LB}	Quality factor	Measured at 700 MHz at 2 V	55	65		
Q _{HB}	Quality factor	Measured at 2700 MHz at 2 V	35	50		
IP3	Third order intercept point	V _{bias} = 1 V ⁽²⁾⁽⁴⁾	52	60		dPm
IF 3	Trilla order intercept point	$V_{\text{bias}} = 24 \ V^{(2)(4)}$		75		ubiii
H2	Second harmonic	$V_{\text{bias}} = 1 \ V^{(3)(4)}$		-65	-45	dBm
112	Second Harmonic	$V_{\text{bias}} = 24 \ V^{(3)(4)}$		-75		ubiii
H3	Third harmonic	V _{bias} = 1 V ⁽³⁾⁽⁴⁾		-35	-30	dBm
113	Trilla Harmonic	$V_{\text{bias}} = 24 \ V^{(3)(4)}$		-65		UBIII
+	Transition time	Average for any transition between C _{min} to C _{max} ⁽⁵⁾		40		
t _T	Transition time	Average transition between C _{max} to C _{min} ⁽⁵⁾		20		μs

^{1.} Measured at low frequency

^{2.} F_1 = 894 MHz, F_2 = 849 MHz, P_1 = +25 dBm, P_2 = +25 dBm, $2f_1$ - f_2 = 939 MHz

^{3. 850} MHz, P_{in} = +34 dBm

^{4.} IP3 and harmonics are measured in the shunt configuration in a 50 $\boldsymbol{\Omega}$ environment

^{5.} One or both of ${\rm RF_{in}}$ and ${\rm RF_{out}}$ must be connected to DC ground, using the HVDAC turbo mode

Electrical characteristics STPTIC-56G2

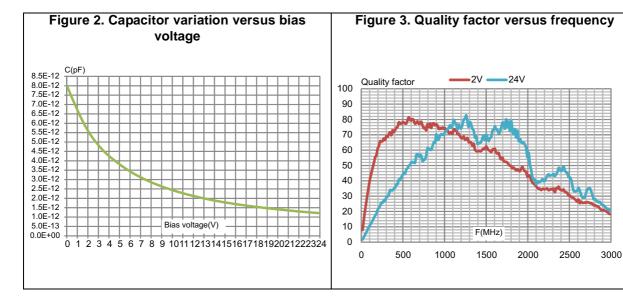
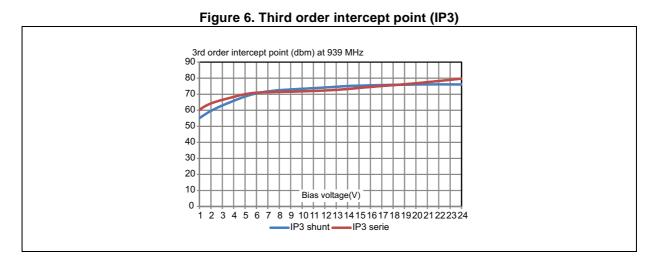


Figure 4. Harmonic power versus bias voltage Figure 5. Harmonic power versus bias voltage (series) (shunt) 0 Harmonic power (dbm) pin = +34dbm at 850 MHz Harmonic power (dbm) pin = +34dbm at 850 MHz -10 -10 -20 -20 -30 -40 -40 -50 -50 -60 -60 -70 -80 -80 Bias voltage(V) Bias voltage(V) -90 -90 0 1 2 3 4 5 6 7 8 9 1011 12131415161718192021222324 0 1 2 3 4 5 6 7 8 9 1011 12131415161718192021222324 H2 serie H3 serie H2 shunt —H3 shunt



STPTIC-56G2 Package information

2 Package information

- Epoxy meets UL94, V0
- Lead-free package

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

2.1 Flip-Chip package information

Bottom view Top view Side view (balls dow) (balls up) C2 A2 D3 D2 D1 В1 BIAS E1 B2 Α1 E2 B4 C2 NC1 <

Figure 7. Flip-Chip package outline

The land pattern below is recommended for soldering the STPTIC-G2 on PCB.

NC stands for No Connect, this pad must not be connected on application board. Please leave this pad floating.

Dimensions (micron)	A 1	A2	B1	B2	В4	C1	C2	D1	D2	D3	E1	E2
STPTIC-15/27/33/39/47G2	640				120							
STPTIC-56G2	710	590	120	400	190	85	420	200	90	290	125	165
STPTIC-68G2	780	390	120	400	260	65	420	200	90	290	123	105
STPTIC-82G2	880				360							
Tolerance	±30	±30	±15	±10	±15	±15	±10	±20	±20	±40	±20	±20

Table 4. Flip-Chip package dimensions

Package information STPTIC-56G2

X1 Copper—→ W1 L2 L1 L3 X2 nask opening (25 μm) largeur than copper

Figure 8. Recommended PCB land pattern for Flip-Chip package

Table 5. Dimensions

Dimensions	L1	W1	L3	L2	W2	L4	X1	X2	Y1	Y2
Typical values (micron)	160	160	260	210	210	310	320	270	240	190

Packing information 2.2

Figure 9. Flip-Chip tape and reel outline

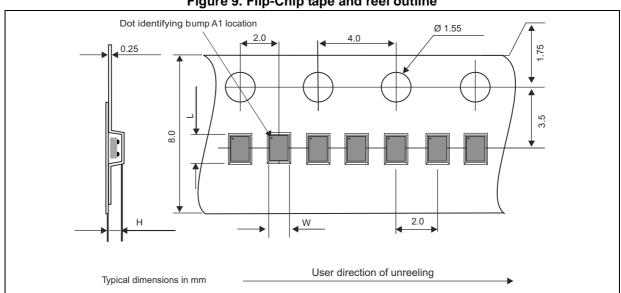


Table 6. Dimensions

Pocket dimensions	L	w	н
STPTIC-15/27/33/39/47G2	730	680	380
STPTIC-56G2	800	680	380
STPTIC-68G2	870	680	380
STPTIC-82G2	970	680	380



STPTIC-56G2 Package information

Figure 10. Flip-Chip marking

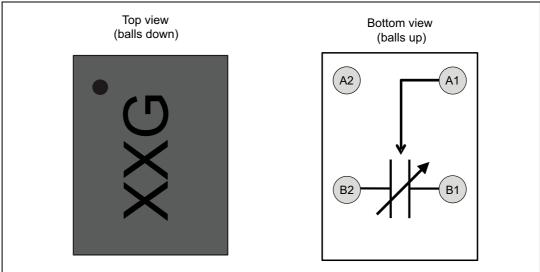


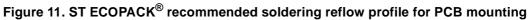
Table 7. Pinout description

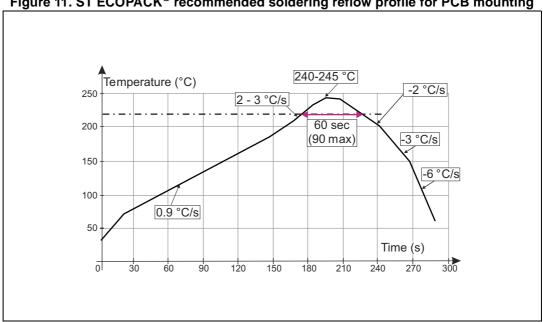
Pad / ball number	Pin name	Description
A1	DC bias	DC bias voltage
B1	RF2	RF input / output ⁽¹⁾
A2	NC	Not connected
B2	RF1	RF input / output

^{1.} When connected in shunt, please connect RF2 (B1 ball) to GND

Reflow profile STPTIC-56G2

Reflow profile 3





Note: Minimize air convection currents in the reflow oven to avoid component movement.

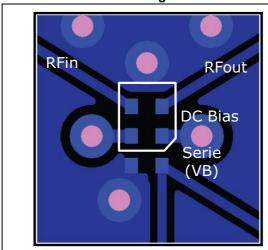
Table 8. Recommended values for soldering reflow

Profile	Value			
Fiolile	Typical	Max.		
Temperature gradient in preheat (T = 70-180 °C)	0.9 °C/s	3 °C/s		
Temperature gradient (T = 200-225 °C)	2 °C/s	3 °C/s		
Peak temperature in reflow	240-245 °C	260 °C		
Time above 220 °C	60 s	90 s		
Temperature gradient in cooling	-2 to -3 °C/s	-6 °C/s		
Time from 50 to 220 °C	160 to 220 s			

STPTIC-56G2 Evaluation board

4 Evaluation board

Figure 12. Series and shunt connection



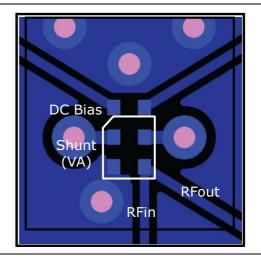


Figure 13. Layer 1 and layer 4

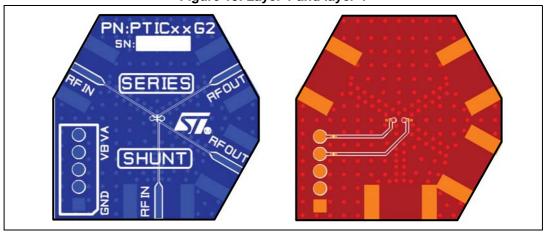
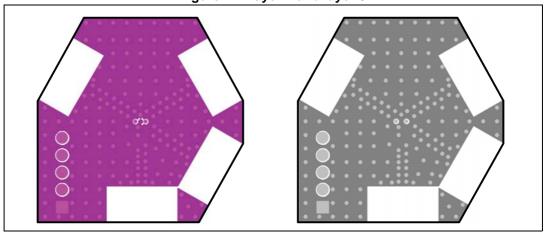


Figure 14. Layer 2 and layer 3



Ordering information STPTIC-56G2

5 Ordering information

Figure 15. Ordering information scheme

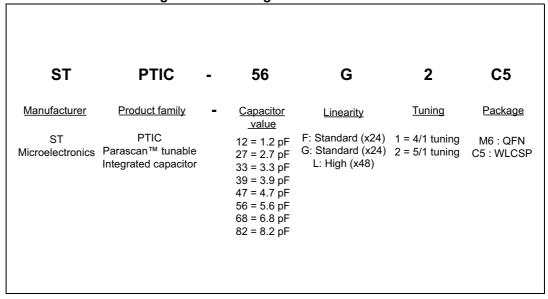


Table 9. Ordering information

Part number	Marking	Base qty	Package	Delivery mode
STPTIC-56G2C5	56G	15 000	Flip-Chip	Tape and reel

6 Revision history

Table 10. Document revision history

Date	Revision	Changes
23-Jul-2015	1	Initial release.

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