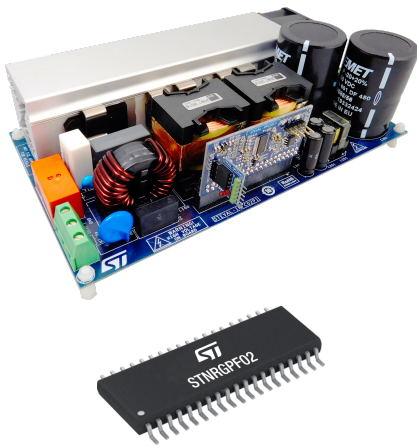


2 kW two-channel interleaved PFC reference design based on the STNRGPF02 digital controller



Features

- Input voltage range: 90 to 265 V_{AC}
- Line frequency range: 47 to 63 Hz
- Maximum output power: 2 kW at 230 V
- Inrush current limiter
- Output voltage: 400 V
- Power factor: > 0.98 at 20% load
- Total harmonic distortion: <5% at 20% load
- Mixed-signal average current mode control, CCM fixed frequency operation
- Switching frequency (fsw): 60 kHz
- Cycle-by-cycle regulation (analog current control loop)
- Input voltage and load feed-forwards
- Phase shedding
- Current balance
- Burst-mode operation
- Overvoltage protection
- Overcurrent protection
- Thermal protection
- Status indicator LEDs
- Cooling function

Product summary

| | |
|--|--|
| 2 kW two-channel interleaved PFC based on the STNRGPF02 digital controller | STEVAL-IPFC02V1 |
| 2 kW two-channel interleaved PFC based on the STNRGPF02 digital controller | STNRGPF02 |
| trench gate field-stop IGBT | STGW20H65FB |
| power Schottky silicon carbide diode | STPSC12065D |
| Application | PFC Converter - Single Phase Input |
| Articles | Digital PFC blog article |

Description

The [STEVAL-IPFC02V1](#) 2 kW interleaved PFC reference design features the performance of analog cycle-by-cycle current regulation and the flexibility of digital control to generate sinusoidal supplies with very high power factor and very low harmonic distortion.

Digital power control is based on the [STNRGPF02](#) digital PFC controller, which can drive up to two interleaved PFC channels using mixed signal (analog and digital) average current mode control in CCM at fixed frequency.

The 2 kW interleaved PFC reference design consists of a power board with 2-ch interleaved CCM boost power stage, auxiliary power supply, a control board with embedded [STNRGPF02](#) digital controller and a small adapter board for programming the [STNRGPF02](#).

eDesignSuite is the tool available in the ST website to configure the [STNRGPF02](#) according to specific design requirements for each interleaved PFC.

1 Design overview: 2 kW 2-ch interleaved PFC

The aim of this reference design is to provide a flexible PFC converter that can accept a wide input range (90 to 265 V at 50/60 Hz) for high power applications (higher than 600 W) that require supply power with very high PF and very low THD, in an efficient and cost effective package that can be easily configured for specific performance criteria.

The flexibility of programmable digital control and the high performance of analog logic render the **STNRGPF02** digital controller as the ideal choice, specifically designed for interleaved CCM boost PFC for applications above 600 watts.

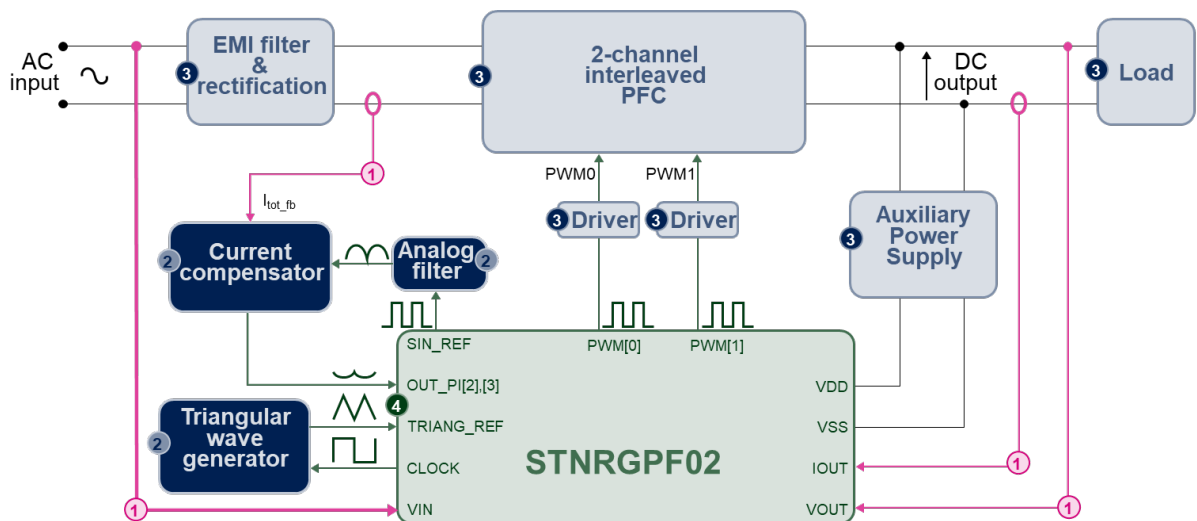
STNRGPF02 implement a mixed signal (analog/digital) control offering the advantages of very high end digital solution without typical limits of analog ones.

The inner current loop is performed in hardware realizing an analog Proportional-Integral (PI) compensator, ensuring regulation cycle by cycle. The outer voltage loop is performed by a digital PI controller .

Moreover the digital section includes an input voltage and load feedforward for fast transient response when main voltage changes suddenly or a load step current occurs.

Figure 1. STEVAL-IPFC02V1 block diagram

1. I/O measurement signals
2. Analog circuitry
3. Power stages
4. Digital control section



The PFC stage is based on a boost circuit design with two parallel channels to take advantage of the controller's ability to support interleaving through a secondary PWM channel that is phase-shifted 180° with respect to the master channel. While two channels increase circuit complexity, the interleaving operation ensures that there is less ripple and higher apparent switching frequency in the PFC input current, which allow the use of smaller and less expensive input EMI filters, boost inductors and switching devices.

The **STGW20H65FB** IGBTs used for the boost switches are cost effective devices especially designed to minimize losses in power converters thanks to their low $V_{CE(sat)}$ and reduced tail current profile.

2 Schematic diagrams

Figure 2. STEVAL-IPFC02P1 schematic - input section

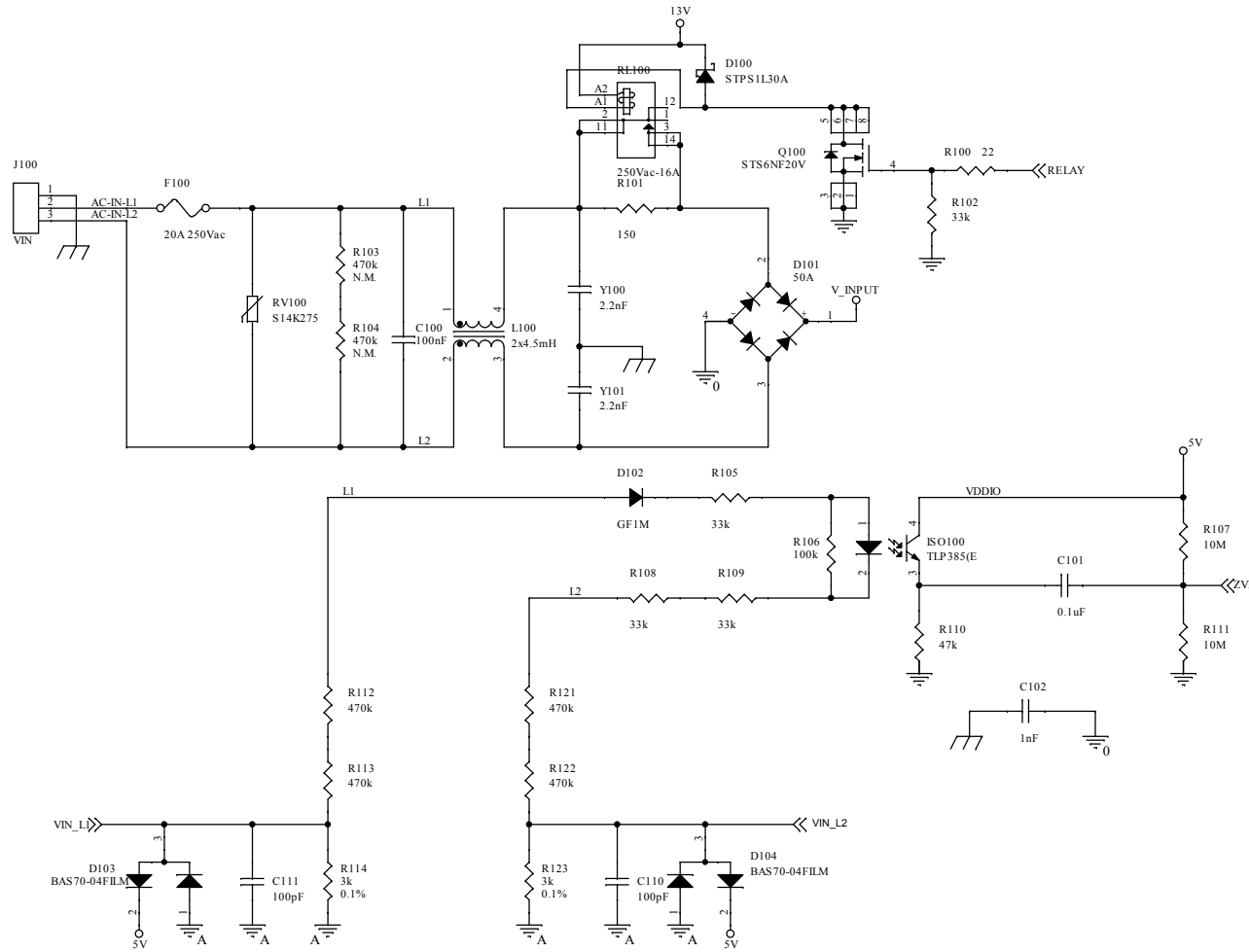


Figure 3. STEVAL-IPFC02P1 schematic - auxiliary power supply

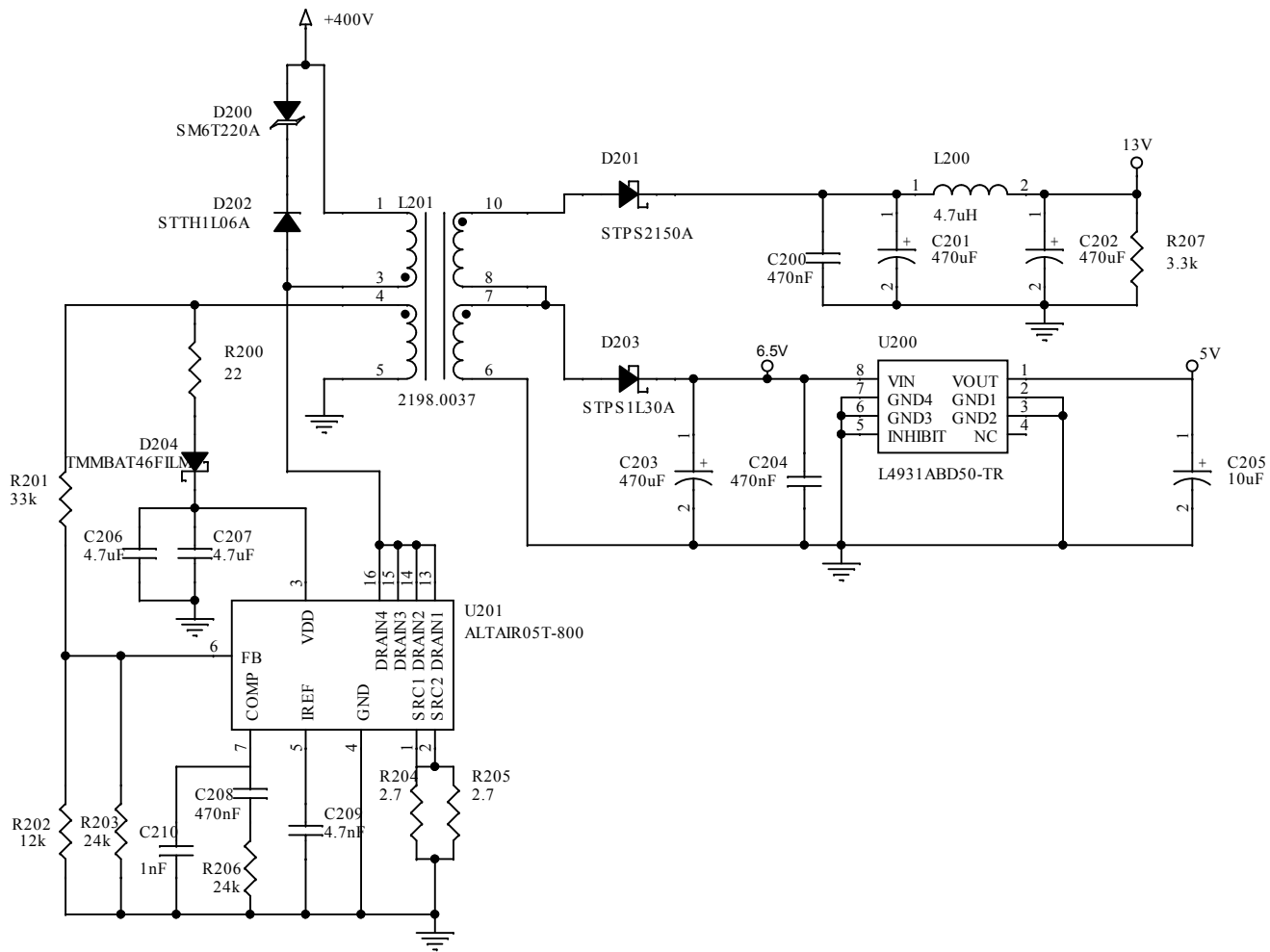


Figure 4. STEVAL-IPFC02P1 schematic - boost interleaving section

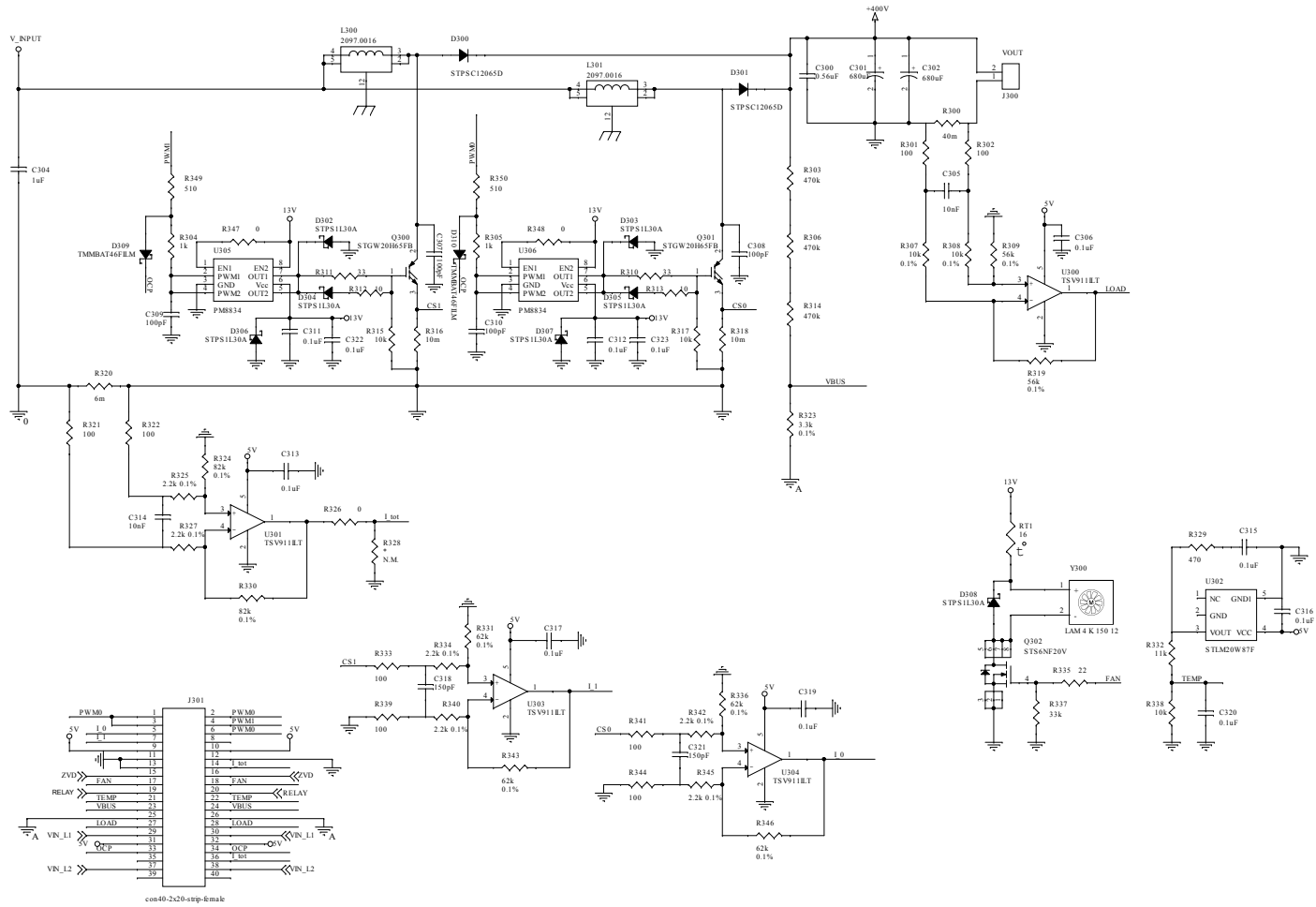


Figure 5. STEVAL-IPFC02C1 schematic

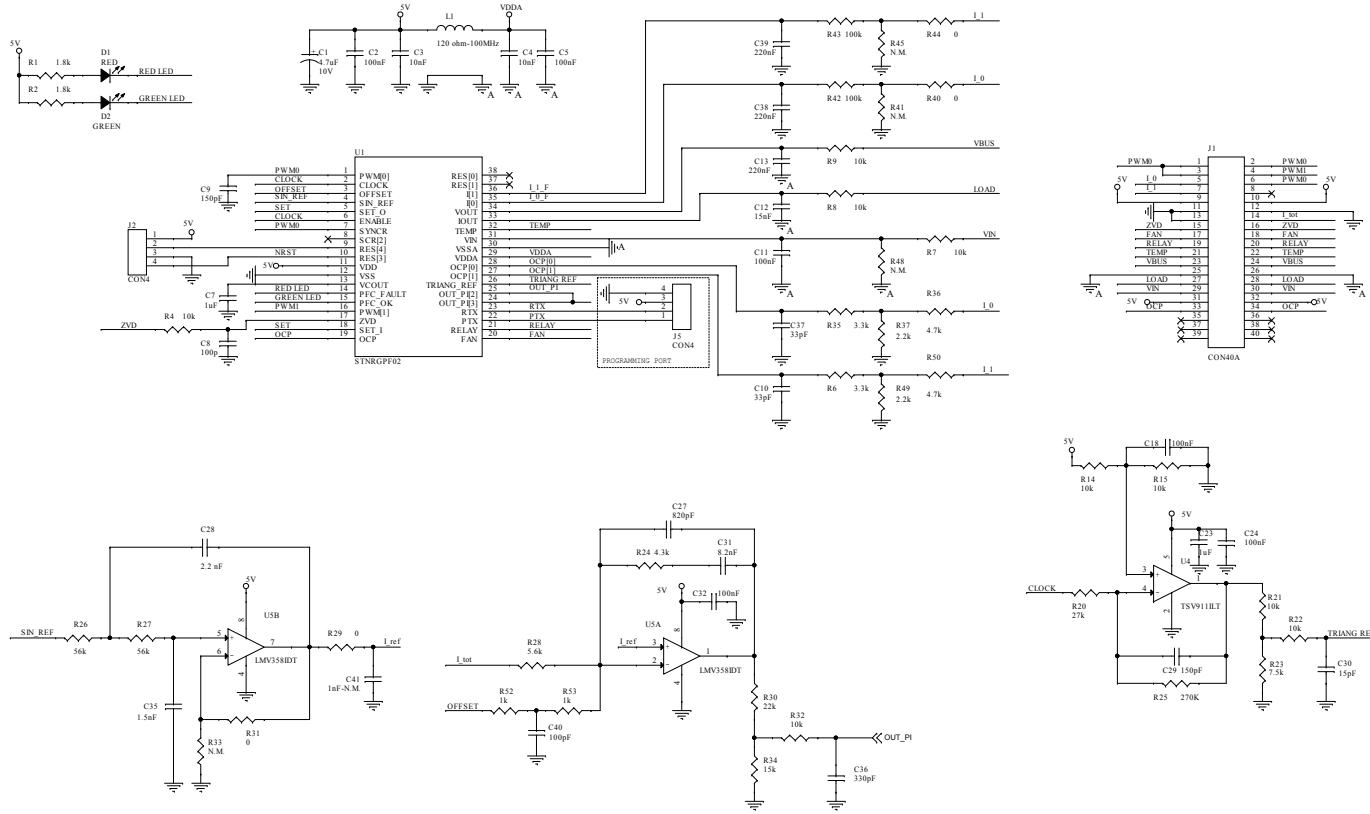
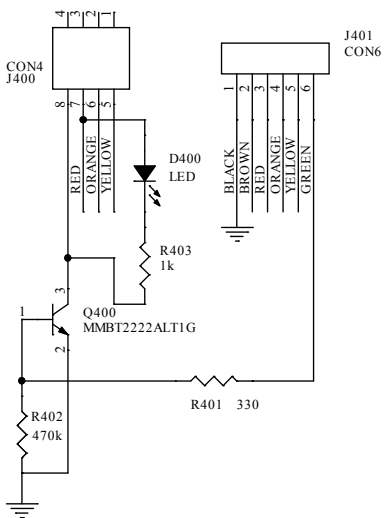


Figure 6. STEVAL-IPFC01A1 schematic



Revision history

Table 1. Document revision history

| Date | Version | Changes |
|-------------|---------|------------------|
| 09-Mar-2020 | 1 | Initial release. |

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, please refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2020 STMicroelectronics – All rights reserved